

### Abstract of the Disclosure

A semiconductor memory device having a bitline coupling scheme capable of preventing sensing speed from lowering due to variations in an external power supply is provided. The semiconductor memory device includes a memory cell array which includes a plurality of memory cells, a bitline and a complementary bitline which are connected to the memory cell array, a coupling capacitor one end of which is connected to either the bitline or the complementary bitline and the other end of which a control signal is applied to, a bitline sensing amplifier which senses and amplifies a difference in the voltage between the bitline and the complementary bitline, and a control circuit which generate the control signal. Here, an internal power supply generated by dropping an external power supply applied from the outside of the semiconductor memory device is used as a power supply of the control circuit.

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